Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1A**
2. **1B**
3. **1Y**
4. **2A**
5. **2B**
6. **2Y**
7. **GND**
8. **3Y**
9. **3A**
10. **3B**
11. **4Y**
12. **4A**
13. **4B**
14. **VCC**

**1 14**

**2**

**3**

**4**

**5**

**6**

**7**

**13**

**12**

**11**

**10**

**9**

**8**

**MASKREF**

**.041”**

**.033”**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .0029” X .0029”**

**Backside Potential: GND (or leave FLOATING)**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .033” X .041” DATE: 8/18/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .029” P/N: 54LVC32A**

**DG 10.1.2**

#### Rev B, 7/19/02